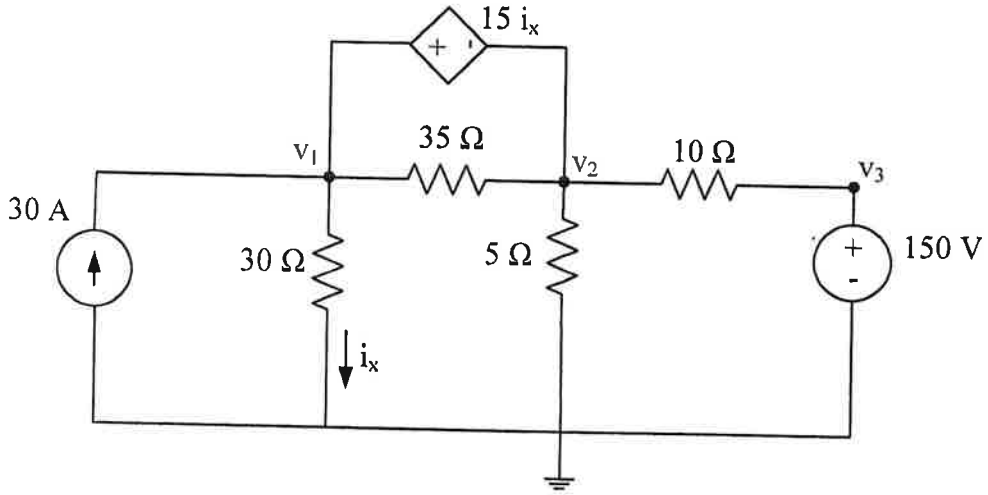
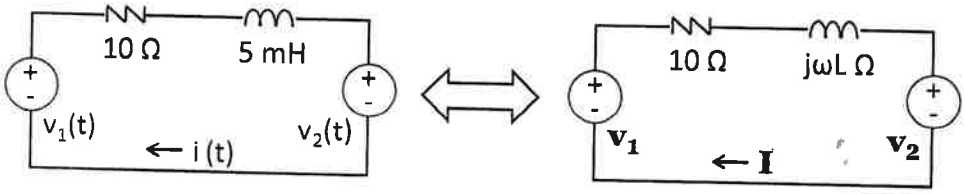
Problem : P1 **Area** **Circuits and Electronics** **Student Code____**

Solve for the node voltages, v_1, v_2 and v_3 in the following circuit.



Problem : P2 **Area Circuits & Electronics** **Student Code_____**

Determine the phasor I and the steady-state i(t) for the following three cases utilizing the superposition theorem.



(Time domain) (Phasor domain)

(1) $v_1(t) = 5\cos(2{,}000t)$ [V], $v_2(t) = 10$ [V]:
(2) $v_1(t) = 5\cos(2{,}000t)$ [V], $v_2(t) = 10\cos(2{,}000t + 60)$ [V]:
(3) $v_1(t) = 5\cos(2{,}000t)$ [V], $v_2(t) = 10\cos(4{,}000t + 60)$ [V]:

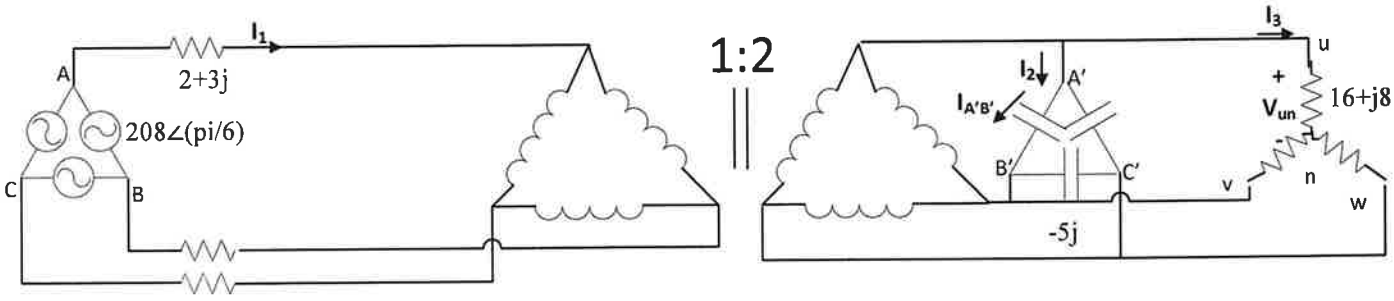
Problem: P6 Area: Communications/Signal Processing Student Code:

Given the difference equation $y[n]+3y[n-1]+5y[n-2]=3x[n]-x[n-1]$, calculate the z-transform Y(z) if $x[n]=\delta[n]$ and the initial conditions are all zero except for $x[-1]=3$. Identify which portion of Y(z) corresponds to the stored energy response of the system.

Problem: 14 **Area: Power** **Student Code: _____**

In the following circuit, find the following (both amplitude and angle):

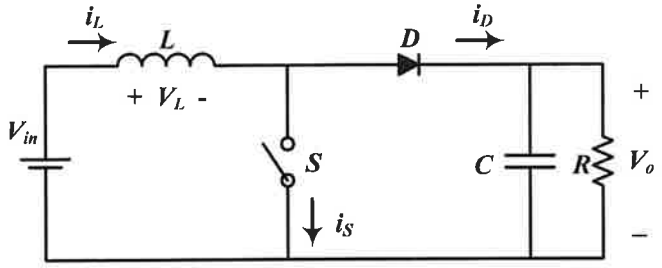
a) I_1, I_2, and I_3 (60 points).
b) $I_{A'B'}$ (Capacitor current in the original delta form) (20 points)
c) 3-phase complex power of the source (20 points)



Problem: 15 **Area: Power** **Student Code:_____**

A Boost dc-dc converter has the following parameters: V_{in} = 100 V, d = 0.5, L = 800 μH, and f_{sw} = 100 kHz. Start from steady state.

C = infinity, R = 100.



a) Find the maximum and minimum value of the inductor current.

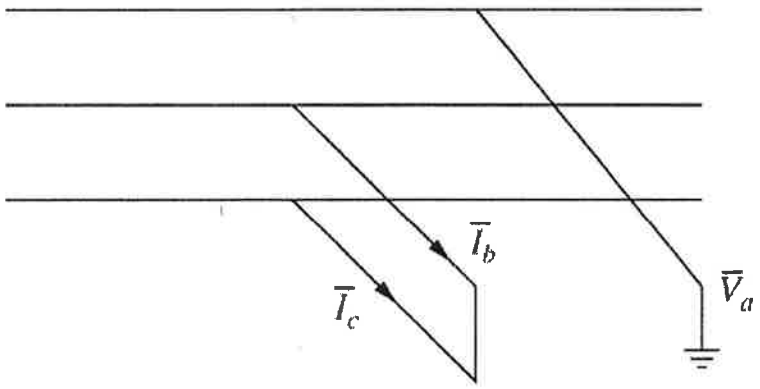
b) Accurately plot the waveform of the inductor current.

c) Find the average value of the switch current.

d) Find the input power.

Problem: 16 **Area: Power** **Student Code:_____**

At the general three-phase bus shown in the below figure, consider a simultaneous single line-to-ground fault on phase a and line-to-line fault between phases b and c, with no fault impedances. Obtain the sequence-network interconnection satisfying the current and voltage constraints.



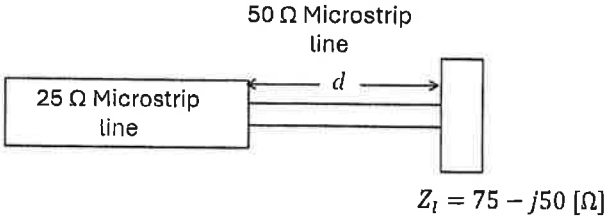
Fault conditions

Problem: 19 **Area: Waves and Devices** **Student Code____**

1. A lossless microstrip line with a characteristic impedance of 50 Ω and a length of d meets a load impedance of $Z_L = 75 - j50$ Ω on the right, and a second microstrip line with a characteristic impedance of 25 Ω on the left. A top view is shown below.

a. Assume that $d = 3$ cm, the frequency is 5 GHz, and the effective relative permittivity of the 50 Ω microstrip line is 1.75. Find the load impedance seen by the 25 Ω microstrip line. Use $Z_{in} = Z_0\,(Z_L + jZ_0 \tan \beta d)/(Z_o + jZ_L \tan \beta d)$.

b. Find the SWR seen on the 25 Ω microstrip line.



Problem: 21 **Area**: Computational Intelligence **Code #**_____

Answer the questions for parts a-c below.

a) Define supervised and unsupervised learning. Give an example of a computational intelligence algorithm that utilizes each learning approach.

b) What is Reinforcement Learning (RL)? Explain with an aid of a diagram. Give two examples of applications where reinforcement learning is a more appropriate computational learning approach than supervised or unsupervised learning.

Problem: 22 **Area**: Computational Intelligence **Code #**_____

Answer the questions for parts a and b below.

a) In developing an optimal multilayer perceptron with the back-propagation algorithm, what variable parameters have to be decided upon? Explain the purpose of each parameter in the back-propagation algorithm.

b) Radial-basis function (RBF) networks and multilayer perceptrons (MLPs) are examples of nonlinear layered feedforward networks. They are both universal approximators. However, these two networks differ from each other in several important ways. Mention at least **three** differences.

Problem: 24 **Area**: Computational Intelligence **Code #**_____

Answer the questions for parts a and b below.

(a) What are Ontogenic neural networks?

(b) What is the difference between a recurrent neural network (RNN) and a simultaneous recurrent network (SRN)?

Problem: 25 **Area**: Computer Architecture/Embedded Systems **Code #**_____

Consider the following data for the execution of given instruction sequence of 10 million instructions in different processors.

Processor	Clock Rate	CPI
P1	2GHz	1.25
P2	1.5GHz	0.75

a. Calculate **CPU execution time** for P1 and P2. Which one is better in terms of CPU execution time?

b. Calculate **MIPS** (Millions of instructions per second) for P1 and P2. Which one is better in terms of MIPS?

Problem: 26 **Area**: Computer Architecture/Embedded Systems **Code #**_____

Suppose you are given a simple memory hierarchy with a **direct-mapped** cache memory which can store **8 one-word data blocks** and a **word-addressable** main memory which can store **16 data words**. For a word address sequence of 0000, 1000, 0000, 1000, 1100, 0100 and 1100 in binary, **complete the following table** by showing: tag, index, hit/miss and cache contest after each access. Then, **calculate its hit ratio**.

Addr	Tag	Index	Hit/ Miss	Cache content after access							
				000	001	010	011	100	101	110	111
0000											
1000											
0000											
1000											
1100											
0100											
1100											

Hit ratio =_____

Suppose you are given a simple memory hierarchy with a **4-way set associative** cache memory which can store **8 one-word data blocks** and a **word-addressable** main memory which can store **16 data words**. For a word address sequence of 0000, 1000, 0000, 1000, 1100, 0100 and 1100 in binary, **construct a table** to show: tag, index, hit/miss and cache contest after each access. Use **LRU (Least Recently Used)** replacement strategy. Then, **calculate its hit ratio**.

Problem: 28 **Area**: Computer Architecture/Embedded Systems **Code #**_____

Define Harvard and Von Neumann architectures. Give examples of processors that are designed using a Harvard architecture and using a Von Neumann architecture.

Problem: 29 **Area**: Integrated Circuits and Logic Design **Code #**_____

Given the truth table shown, implement the function F(A,B,C,D) using:

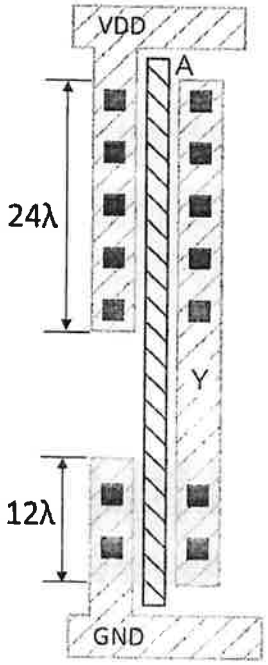
a) a 4:1 Mux plus any other additional basic logic gates

A B C D	F
0 0 0 0	1
0 0 0 1	0
0 0 1 0	0
0 0 1 1	1
0 1 0 0	0
0 1 0 1	0
0 1 1 0	1
0 1 1 1	1
1 0 0 0	0
1 0 0 1	1
1 0 1 0	1
1 0 1 1	1
1 1 0 0	0
1 1 0 1	0
1 1 1 0	0
1 1 1 1	1

b) two 3x8 Active-Low Decoders with ACTIVE-LOW enables and outputs.

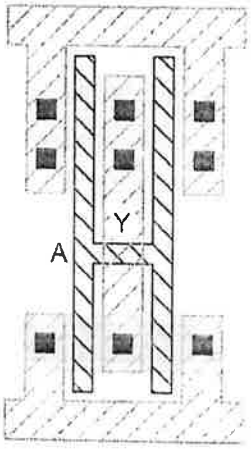
Problem: 30 **Area**: Integrated Circuits and Logic Design **Code #**_____

a. Sketch a transistor-level schematic of the below layout and annotate the transistor with its width.



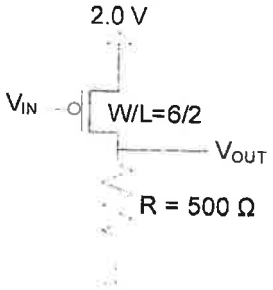
b. When a unit (4λ) transistor has diffusion capacitance C, calculate the total diffusion capacitance at the output node Y.

c. When the layout in (a) is folded as shown below, calculate the total diffusion capacitance at the output node Y.



Problem: 31 **Area**: Integrated Circuits and Logic Design **Code #**_____

For the simple inverter shown below, Vin = 1.0 V. Find Vout. The FET characteristics are given in the table below.



	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

Problem: 32 **Area**: Integrated Circuits and Logic Design **Code #**_____

Find the minimal SOP expression for f, which is given as:

$f(w,x,y,z) = (w + y' + z)(w' + x + y' + z')(w' + x' + y' + z)(x + y' + z')(w' + x' + y' + z)(w' + x' + y' + z')$

Problem: P33 **Area: Networking, Security, and Dependability** **Student Code:**

This problem has two parts. For full credit, you must answer both correctly. Show your work for any answer that involves computation.

Part 1. Answer all four questions below.

a. Describe two complications that would arise if we redesigned IP to directly use MAC addresses instead of IP addresses. The redesign would eliminate the need to use ARP to look up the MAC address because the IP and MAC address for each interface would have the same value.

b. Why does IP tolerate point-to-point interfaces that have non-unique addresses?

c. If you know the MAC address of one interface of a host, can you predict any part of the MAC address of a different interface on the same host? Why or why not?

d. The ID field in the IPv4 header has a fixed length. As a result, we have a limited number of unique datagrams IDs available for IP datagrams. This shortage of unique IDs was one problem that led IPv4 to be replaced by IPv6. Explain why shortage of datagram IDs is almost never a problem for IPv4.

Part 2. Assume that you are the administrator of an ISP. You have a 128.20.224.0/20 address block. No additional IP addresses can be acquired.

a. How many usable host addresses are available in this address block?

b. Identify the first and last addresses in the block. Represent each in dotted decimal notation.

c. You have two customers, A and B, with 1000 hosts each; two customers, C and D, with 500 hosts each; and three customers, E, F, and G, with 250 hosts each.

d. Your task is to identify non-overlapping address blocks that will provide each customer with one contiguous block of IP addresses that is large enough to allow them to assign a unique address to each of their hosts. Use notation similar to 128.20.224.0/20 to show the address block for each customer.

Note: 20D = 14H, 128D = 80H, 224D = E0H.

Problem: P34 **Area: Networking, Security, and Dependability** **Student Code:**

This problem has four parts. For full credit, you must answer all four parts correctly. Show your work for any answer that involves computation.

A hypothetical error-detecting scheme uses one parity bit, P_1, for checking all data bits in odd-numbered positions; and a second parity bit, P_2, for checking data bits in even-numbered positions. For example, assuming the choice of even parity, the codeword corresponding to the message 111011 is 11101110, and determined as follows:

Value of bit:	1 1 1 0 1 1 1 0	P_1 checks the parity of bits in positions 1, 3, and 5
Position of bit:	1 2 3 4 5 6 P_1 P_2	P_2 checks the parity of bits in positions 2, 4, and 6

Part 1. How many single-bit errors can this scheme claim to detect and correct, respectively? Justify your answers and explain whether each of them depends on the length of the message (which is six in this example).

Part 2. What is the minimum Hamming distance of this code? Justify your answer.

Part 3. Assume a bit error rate of p, independence among bit errors, and the more general case where each message is m bits long. Using the scheme described above, what is the probability of receiving a code word (message and parity bits) that has at least one bit in error? Recall that this probability is the frame error rate and addresses the probability of existence of bit errors, not the probability of detecting these errors.

Part 4. Does the presence of P_1 and P_2 change the frame error rate you calculated in part 3? In other words, is the frame error rate for the $(m + 2)$-bit code word calculated with the hypothetical scheme described above the same as the frame error rate for an $(m + 2)$-bit data stream where all bits are data bits and no error detection has been applied? Answer carefully and justify your answer.